RECEIVED
CENTRAL FAX CENTER

AUG 3 0 2006

PATENT APPLICATION

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

ATTORNEY DOCKET NO. 10016615-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Leith Johnson

Application No.: 10/017,371

Filing Date: 12/7/01

Confirmation No.: 8105

Examiner: Sheng Jen Tsai

Group Art Unit: 2186

Title: Virtualized Resources in a Partitionable Server

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on July 13, 2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

☐ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450

Date of Deposit:

OR

☒ I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (571)273-8300.

Date of facsimile: August 30, 2006

Typed Name: Robin A. Matachun

Signature:

Respectfully submitted,

Leith Johnson

By

Robert Plotkin, Esq.

Attorney/Agent for Applicant(s)

Reg No.: 43,861

Date: August 30, 2006

Telephone: 978-318-9914

08/31/2006 TLO111 00000009 082025 10017371

01 FC:1402 500.00 DA

Rev 10/05 (ApiBrief)

RECEIVED
CENTRAL FAX CENTER

AUG 30 2006

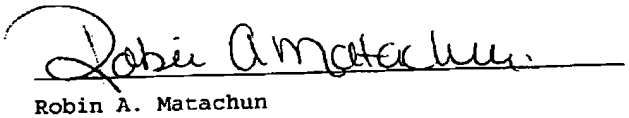
ATTORNEY'S DOCKET NO: 10016615-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leith Johnson
Serial No:	10/017,371
Filed:	December 7, 2001
For:	Virtualized Resources in a Partitionable Server
Examiner:	Sheng Jen Tsai
Art Unit:	2186

CERTIFICATE OF TRANSMISSION BY FACSIMILE

The undersigned hereby certifies that the correspondence listed above is being transmitted to the Commissioner for Patents by facsimile via facsimile number 571-273-8300 on August 30, 2006.



Robin A. Matachun

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF ON APPEAL

This is an appeal pursuant to 35 U.S.C. § 134 from the Examiner's decision rejecting claims 1-5, 8-11, 14-21, 23, 25, and 27-31 as set forth in the Final Office Action of March 13, 2006, and as maintained in the Advisory Action of June 6, 2006.

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having its principal place of business in Houston, Texas.

RELATED APPEALS AND INTERFERENCES

Applicant's attorney knows of no related pending appeals or interferences.

STATUS OF CLAIMS

Claims 1-5, 8-11, 14-21, 23, 25, and 27-31 are pending in this application.

Claims 1-5, 8-11, 14-21, 23, 25, and 27-31 stand rejected and are the subject of this appeal. More specifically, claims 1-5, 8-11, 14-21, 23, 25, and 27-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gulick et al. (U.S. Pat. No. 6,314,501) in view of Vishin et al. (U.S. Pat. No. 5,860,146).

STATUS OF AMENDMENTS

Remarks, but no amendments, were submitted in an after-final response on May 15, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

Claims 1-5, 8-11, and 27-28 all include substantially the same relevant limitations related to creating a physical resource identifier space in a partition of a partitionable computer system. In particular, all of these claims include limitations requiring a mapping that defines a non-monotonic function. The relevance of this limitation will be explained in more detail below.

Table 1 shows the preamble and elements of independent claim 1, and examples of where support for the text of claim 1 may be found in the specification.

Claim Text	Support in Specification
Claim 1. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers,	P. 12, lines 18-31; FIGS. 3A-3B (showing examples of machine resources); p. 13, line 20 - p. 15, line 23); FIG. 2C (machine memory blocks 210a-e); p. 16, lines 15-31 (machine addresses 216 are examples of "machine resource identifiers"); and FIGS. 6A-6B (machine resource identifiers 616a-g); p. 36, line 9 - p. 37, line 3.

a method for creating a physical resource identifier space in a partition of the partitionable computer system, the method comprising steps of:	FIG. 4; p. 22, line 20 - p. 25, line 3.
establishing a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers,	FIG. 4, steps 406-416; p. 23, line 6 - p. 24, line 8 (the physical-to-machine address translation table is an example of a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers).
wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero,	P. 12, lines 9-10; FIGS. 2A-2B (physical address spaces 202a-b); p. 15, lines 30-32; and p. 17, lines 7-11, 22-28.
and wherein the mapping defines a non-monotonic function; and	FIGS. 2A-2C (e.g., mapping between physical addresses 218a and the corresponding portion of machine addresses 216).
(B) providing, to an operating system executing in the partition, an interface for the operating system to access the at least some of the plurality of machine resources using the plurality of physical resource	FIGS. 2A-2B (the virtual-to-physical translation mechanisms 204a-b are examples of interfaces to operating systems); p. 15, line 33 - p. 16, line 14.

identifiers.	

Table 1: Claim 1

Independent claim 8 contains substantially similar limitations, which find support in at least the same places in the specification.

Claims 14-21 and 29 all include substantially the same relevant limitations related to accessing a physical machine resource in a partitionable computer system. In particular, all of these claims include limitations requiring a mapping that defines a non-monotonic function. Table 2 shows the preamble and elements of independent claim 14, and examples of where support for the text of claim 14 may be found in the specification.

Claim Text	Support in Specification
Claim 14. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers,	p. 12, lines 18-31; FIGS. 3A-3B (showing examples of machine resources); p. 13, line 20 - p. 15, line 23); FIG. 2C (machine memory blocks 210a-e); p. 16, lines 15-31 (machine addresses 216 are examples of "machine resource identifiers"); and FIGS. 6A-6B (machine resource identifiers 616a-g); p. 36, line 9 - p. 37, line 3.
a method for accessing a select	FIG. 5; p. 25, line 3 - p. 26,

one of the plurality of machine resources specified by a physical resource identifier provided by an operating system executing in a partition in the partitionable computer system, the method comprising steps of:	line 9.
(A) identifying a mapping associated with the partition, wherein the mapping maps a plurality of physical resource identifiers in a sequential zero-based physical resource identifier space of the partition to at least some of the plurality of machine resource identifiers, and wherein the mapping defines a non-monotonic function;	FIG. 5, element 504; p. 25, lines 27-29; and FIGS. 2A-2C (e.g., mapping between physical addresses 218a and the corresponding portion of machine addresses 216).
(B) translating the physical resource identifier into a machine resource identifier using the mapping, wherein the machine resource identifier specifies the select one of the plurality of machine resources; and	FIG. 5, element 506; p. 25, lines 29-32.
(C) causing the select one of the plurality of machine resources to be accessed using the machine resource identifier.	FIG. 5, element 508; p. 25, line 32 - p. 26, line 2.

Table 2: Claim 14

Independent claim 18 contains substantially similar limitations, which find support in at least the same places in the specification.

Claims 23, 25, and 30-31 all include substantially the same relevant limitations related to remapping memory locations, starting from a mapping which defines a non-monotonic function. Table 3 shows the preamble and elements of independent claim 23, and examples of where support for the text of claim 23 may be found in the specification.

Claim Text	Support in Specification
Claim 23. In a partitionable computer system including a plurality of machine memory locations having a plurality of machine addresses,	p. 12, lines 18-31; FIGS. 3A-3B; p. 13, line 20 - p. 15, line 23); and FIG. 2C (machine memory blocks 210a-e); p. 16, lines 15-31.
the partitionable computer system further including a plurality of physical memory locations having a plurality of physical memory addresses that are mapped to at least some of the plurality of machine memory addresses,	FIG. 4, steps 406-416; p. 23, line 6 - p. 24, line 8 (the physical-to-machine address translation table is an example of a mapping between a plurality of physical memory locations and at least some of the plurality of machine memory addresses).
the mapping defining a non-monotonic function,	FIGS. 2A-2C (e.g., mapping between physical addresses 218a and the corresponding portion of

	machine addresses 216).
the partitionable computer system further including a plurality of partitions executing a plurality of software programs, a method comprising steps of:	FIG. 3B (partitions 322a-b execute software programs 330a-d); p. 14, line 26 - p. 15, line 23.
(A) selecting a first subset of the plurality of physical memory locations, the first subset of the plurality of memory locations being mapped to a first subset of the plurality of machine memory addresses; and	FIG. 7, element 702 (physical memory block *P* is a first subset of the plurality of physical memory locations); p. 33, lines 13-28.
(B) remapping the first subset of the plurality of memory locations to a second subset of the plurality of machine memory addresses without rebooting the partitionable computer system.	FIG. 7, elements 704-712; p. 33, line 29 - p. 35, line 17.

Table 3: Claim 23

Independent claim 25 contains substantially similar limitations, which find support in at least the same places in the specification.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The single ground of rejection for review is the rejection of claims 1-5, 8-11, 14-21, 23, 25, and 27-31 under 35 U.S.C. § 103(a)

as being unpatentable over Gulick et al. (U.S. Pat. No. 6,314,501) in view of Vishin et al. (U.S. Pat. No. 5,860,146).

ARGUMENT

The Combination of Gulick and Vishin does not Disclose the Non-Monotonic Function Required by Claims 1-5, 8-11, 14-21, 23, 25, and 27-31

Claims 1-5, 8-11, 14-21, 23, 25, and 27-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gulick et al. (U.S. Pat. No. 6,314,501) in view of Vishin et al. (U.S. Pat. No. 5,860,146). In particular, the Final Office Action asserts that Gulick discloses the limitation, "wherein the mapping defines a non-monotonic function." Applicant respectfully disagrees that Gulick teaches or suggests this limitation, and requests that the rejection be reversed.

The distinction between the claims on appeal and the teachings of Gulick may be made clear by reference to the meaning of "non-monotonic." Merriam Webster's Collegiate Dictionary, 10th Ed., for example, defines "monotonic" as "having the property either of never increasing or of never decreasing as the values of the independent variable or the subscripts of the terms increase." According to this definition, the sequence 1, 2, 5, 10, 10, 10, 16 is monotonic because the values never decrease from one term to the next. Note

that this sequence is monotonic even though all of the values in the sub-sequence 10, 10, 10 are the same. Note further that this sequence is monotonic even though the values of the terms do not increase by equal amounts. This definition of monotonic merely requires that the sequence either never increase or never decrease. In this example, the values of the sequence never decrease and therefore satisfy this definition of "monotonic."

A "non-monotonic" function, therefore, is one which both increases and decreases. For example, the sequence 1, 2, 5, 10, 10, 10, 6 is an example of a non-monotonic function because it both increases (e.g., from 1 to 2) and decreases (e.g., from 10 to 6) from one term to the next.

An example of a non-monotonic mapping function may be found in FIGS. 2A-2C of the present application and the accompanying description. Consider, for example, physical memory blocks 212a, 212e, and 212d, as shown in FIG. 2A. The memory locations in these three memory blocks 212a, 212e, and 212d are sequentially numbered within the physical addresses 218a of the physical address space 202a. Referring to FIG. 2C, however, it may be seen that in the machine address space 202, the machine addresses of physical memory block 212e are *higher* than those of physical memory block 212a, while the machine addresses of physical memory block 212d are *lower* than those of physical memory block 212d. As a result, the mapping

between the physical addresses 218a (FIG. 2A) - containing physical memory blocks 212a, 212e, and 212d - and the corresponding portion of the machine addresses 216 (FIG. 2C) is *non-monotonic*, because as the physical addresses 218a increase, the corresponding ones of the machine addresses 216 first increase, and then decrease.

Neither Gulick nor Vishin, nor the combination thereof, teaches or suggests this express limitation of claim 1, as currently presented. Gulick, for example, teaches a mapping that is monotonic. Referring to FIG. 3 of Gulick, for example, the mapping between the address space labeled "OS#1" and the corresponding addresses in MSU memory space 350 is monotonic. As the addresses in address space OS#1 increase, the corresponding addresses in the MSU memory space 350 *always increase*. Neither Gulick nor Vishin teaches or suggests otherwise.

The Final Office Action incorrectly states that FIG. 33 of Gulick "is a block diagram of apparatus for carrying out the address relocation and reclamation methods of the present invention which leads to a non-monotonic mapping function from physical to machine resources." Gulick uses the term "relocation" merely to refer to the process of mapping addresses in one address space to addresses in another address space. The only examples that Gulick provides of such relocation (mapping) involve monotonic mappings. The Office

Action points to no suggestion in Gulick to create a non-monotonic mapping, and Gulick does not in fact make any such suggestion.

More specifically, FIG. 33 of Gulick illustrates an apparatus for performing the "relocation" and "reclamation" functions described elsewhere by Gulick. As indicated at col. 15, line 66 - col. 16, line 4, Gulick uses the terms "relocated" and "mapped" as synonyms. Gulick defines "relocation" as the "assignment of a base address to an exclusive memory window" (col. 16, lines 19-20). As shown in FIG. 4, operating system window 430 is "relocated" to base address zero, since operating system window 430 is mapped to a portion of the main memory 160 (shown on the right side of FIG. 4) beginning at address zero (col. 16, lines 23-26). Similarly, operating system window 410 is "relocated" to base address 2GB, since operating system window 410 is mapped to a portion of the main memory 160 beginning at address 2GB. The example "relocation" (mapping) shown in FIG. 4 is a *monotonic* mapping.

FIGS. 3 and 5 of Gulick show further examples of the monotonic mappings disclosed by Gulick. More specifically, and as described in more detail in the Response filed by Applicant on February 10, 2006, FIGS. 3 and 5 of Gulick show monotonic mappings between the address spaces labeled "OS#1" and the corresponding addresses in MSU memory spaces 350 and 504, respectively. In summary, the only

mappings disclosed by Gulick are *monotonic* mappings, and Gulick does not suggest using mappings that are non-monotonic.

Gulick also discloses "reclamation," defined as "the re-mapping of the address space within a window in order to reclaim the memory locations that fall behind a memory-mapped I/O address space" (col. 16, lines 30-32). The Advisory Action incorrectly states that Gulick discloses using such reclamation to product non-monotonic mappings. Gulick does not, in fact, teach or suggest performing such reclamation to produce non-monotonic mappings between physical addresses and machine addresses. For example, as described at col. 16, lines 30-59 of Gulick, reclamation is used to reclaim the low memory holes 542 and 572. As shown in FIGS. 3 and 5, however, such reclamation does not produce non-monotonic mappings. Rather, as described above, the mappings between physical and machine addresses shown in FIGS. 3 and 5 are purely monotonic.

The Examiner relies solely on Gulick with respect to the "non-monotonic" claim limitations. The Examiner does not point to any teaching or suggestion in Vishin for the use of non-monotonic mappings.

All of the rejected claims include (either directly or indirectly) the limitation "wherein the mapping defines a non-monotonic function," or a substantially similar limitation. Neither Gulick, nor Vishin, either individually or in combination, teach or

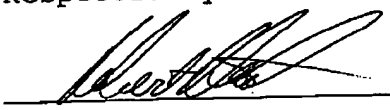
suggest this limitation. The pending claims, therefore, patentably distinguish over the combination of Gulick and Vishin. Applicant therefore traverses the rejection and respectfully requests that it be withdrawn.

CONCLUSIONS

The Examiner's rejections of claims 1-5, 8-11, 14-21, 23, 25, and 27-31 should be reversed for the reasons stated above.

If this Brief is not considered timely filed and if a request for extension of time is otherwise absent, applicant hereby requests any extension of time. Please charge any fees or make any credits, to Deposit Account No. 08-2025.

Respectfully submitted,



August 30, 2006
Date

Robert Plotkin, Esq.
Reg. No. 43,861

Robert Plotkin, P.C.
91 Main Street, Suite 204
Concord, MA 01742-2527
Tel: (978) 318-9914
Fax: (978) 318-9060

APPENDIX A: CLAIMS ON APPEAL

Claim 1. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers, a method for creating a physical resource identifier space in a partition of the partitionable computer system, the method comprising steps of:

(A) establishing a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers, wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero, and wherein the mapping defines a non-monotonic function; and

(B) providing, to an operating system executing in the partition, an interface for the operating system to access the at least some of the plurality of machine resources using the plurality of physical resource identifiers.

Claim 2. The method of claim 1, wherein the plurality of machine resources comprises a plurality of machine memory locations, wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses, and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses.

Claim 3. The method of claim 1, further comprising a step of performing the steps (A) and (B) for each of a plurality of partitions of the partitionable computer.

Claim 4. The method of claim 1, wherein the step (A) comprises a step of creating an address translation table that records the mapping between the plurality of physical resource identifiers and the at least some of the plurality of machine resource identifiers.

Claim 5. The method of claim 1, wherein the interface comprises means for translating a physical resource identifier selected from among the plurality of physical resource identifiers into one of the plurality of machine resource identifiers in accordance with the mapping.

Claim 8. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers, an apparatus comprising:

mapping means for establishing a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers, wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero, and wherein the mapping defines a non-monotonic function; and

interface means for accessing the at least some of the plurality of machine resources in response to requests from an operating system executing in a partition of the partitionable computer system, wherein the requests identify the at least some of the plurality of machine resources using the plurality of physical resource identifiers.

Claim 9. The apparatus of claim 8, wherein the plurality of machine resources comprises a plurality of machine memory locations, wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses, and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses.

Claim 10. The apparatus of claim 8, wherein the mapping means comprises means for creating an address translation table that records the mapping between the plurality of physical resource identifiers and the at least some of the plurality of machine resource identifiers.

Claim 11. The apparatus of claim 8, wherein the interface means comprises means for translating a physical resource identifier selected from among the plurality of physical resource identifiers into one of the plurality of machine resource identifiers in accordance with the mapping.

Claim 14. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers, a method for accessing a select one of the plurality of machine resources specified by a physical resource identifier provided by an operating system executing in a partition in the partitionable computer system, the method comprising steps of:

(A) identifying a mapping associated with the partition, wherein the mapping maps a plurality of physical resource identifiers in a sequential zero-based physical resource identifier space of the partition to at least some of the plurality of machine resource identifiers, and wherein the mapping defines a non-monotonic function;

(B) translating the physical resource identifier into a machine resource identifier using the mapping, wherein the machine resource identifier specifies the select one of the plurality of machine resources; and

(C) causing the select one of the plurality of machine resources to be accessed using the machine resource identifier.

Claim 15. The method of claim 14, wherein the plurality of machine resources comprises a plurality of machine memory locations, wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses, and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses.

Claim 16. The method of claim 14, wherein the step (C) comprises a step of reading a datum from the machine memory address.

Claim 17. The method of claim 14, wherein the step (C) comprises a step of writing a datum to the machine memory address.

Claim 18. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers, an apparatus for accessing a select one of the plurality of machine resources specified by a physical resource identifier provided by an operating system executing in a partition in the partitionable computer system, the apparatus comprising:

means for identifying a mapping associated with the partition, wherein the mapping maps a plurality of physical resource identifiers in a sequential zero-based physical resource identifier space of the partition to at least some of the plurality of machine resource identifiers, and wherein the mapping defines a non-monotonic function;

means for translating the physical resource identifier into a machine resource identifier using the mapping, wherein the machine resource identifier specifies the select one of the plurality of machine resources; and

means for causing the select one of the plurality of machine resources to be accessed using the machine resource identifier.

Claim 19. The apparatus of claim 18, wherein the plurality of machine resources comprises a plurality of machine memory locations, wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses, and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses.

Claim 20. The apparatus of claim 18, wherein the means for accessing comprises means for reading a datum from the machine memory address.

Claim 21. The apparatus of claim 18, wherein the means for accessing comprises a means for writing a datum to the machine memory address.

Claim 23. In a partitionable computer system including a plurality of machine memory locations having a plurality of machine memory addresses, the partitionable computer system further including a plurality of physical memory locations having a plurality of physical memory addresses that are mapped to at least some of the plurality of machine memory addresses, the mapping defining a non-monotonic function, the partitionable computer system further including a plurality of partitions executing a plurality of software programs, a method comprising steps of:

(A) selecting a first subset of the plurality of physical memory locations, the first subset of the plurality of memory locations being mapped to a first subset of the plurality of machine memory addresses; and

(B) remapping the first subset of the plurality of memory locations to a second subset of the plurality of machine memory addresses without rebooting the partitionable computer system.

Claim 25. In a partitionable computer system including a plurality of machine memory locations having a plurality of machine memory addresses, the partitionable computer system further including a plurality of physical memory locations having a plurality of physical memory addresses that are mapped to at least some of the plurality of machine memory addresses, the mapping defining a non-monotonic function, the partitionable computer system further including a plurality of partitions executing a plurality of software programs, an apparatus comprising:

means for selecting a first subset of the plurality of physical memory locations, the first subset of the plurality of memory locations being mapped to a first subset of the plurality of machine memory addresses; and

means for remapping the first subset of the plurality of memory locations to a second subset of the plurality of machine memory addresses without rebooting the partitionable computer system.

Claim 27. The method of claim 1, wherein the interface comprises a Content Addressable Memory that establishes the mapping.

Claim 28. The method of claim 8, wherein the interface means comprises a Content Addressable Memory that establishes the mapping.

Claim 29. The method of claim 18, wherein the means for translating comprises a Content Addressable Memory.

Claim 30. The method of claim 23, further comprising a step of:

(C) prior to the step (B), copying the contents of the first subset of the plurality of machine memory addresses to the second subset of the plurality of machine memory addresses.

Claim 31. The apparatus of claim 25, further comprising:

means for copying the contents of the first subset of the plurality of machine memory addresses to the second subset of the plurality of machine memory addresses.

APPENDIX B: EVIDENCE

No evidence is submitted in support of this Appeal Brief.

APPENDIX C: RELATED PROCEEDINGS

Applicant's attorney knows of no related pending appeals or interferences.